



STP20NM60 - STP20NM60FP STB20NM60 STB20NM60-1

N-CHANNEL 600V - 0.25Ω - 20A TO-220/FP/D²PAK/I²PAK
MDmesh™ Power MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP20NM60	600 V	< 0.29 Ω	20 A
STP20NM60FP	600 V	< 0.29 Ω	20 A
STB20NM60	600 V	< 0.29 Ω	20 A
STB20NM60-1	600 V	< 0.29 Ω	20 A

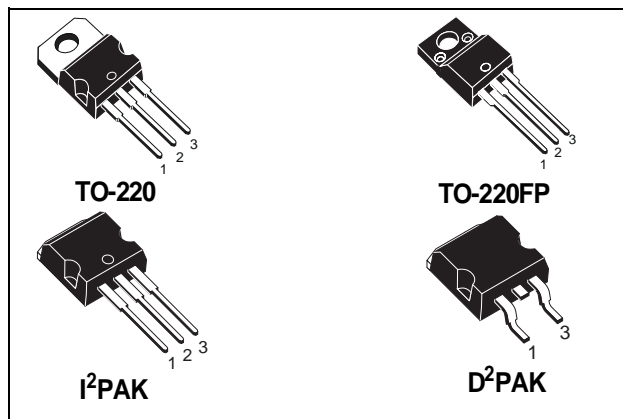
- TYPICAL R_{DS(on)} = 0.25Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE

DESCRIPTION

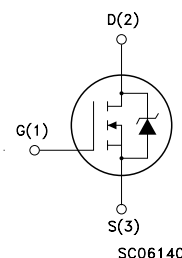
The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.



INTERNAL SCHEMATIC DIAGRAM



SC06140

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP(B)20NM60(-1)	STP20NM60FP	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	600		V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	600		V
V _{GS}	Gate- source Voltage	±30		V
I _D	Drain Current (continuous) at T _C = 25°C	20	20(*)	A
I _D	Drain Current (continuous) at T _C = 100°C	12.6	12.6(*)	A
I _{DM} (●)	Drain Current (pulsed)	80	80(*)	A
P _{TOT}	Total Dissipation at T _C = 25°C	192	45	W
	Derating Factor	1.2	0.36	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	15		V/ns
V _{ISO}	Insulation Withstand Voltage (DC)	--	2500	V
T _{stg}	Storage Temperature	-65 to 150		°C
T _j	Max. Operating Junction Temperature	150		°C

(●) Pulse width limited by safe operating area

(1) I_{SD} ≤ 20A, di/dt ≤ 400A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

(*) Limited only by maximum temperature allowed

STP20NM60 / STP20NM60FP / STB20NM60 / STB20NM60-1**THERMAL DATA**

		TO-220/D ² PAK/I ² PAK	TO-220FP		
Rthj-case	Thermal Resistance Junction-case	Max	0.65	2.8	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	62.5		°C/W
T _l	Maximum Lead Temperature For Soldering Purpose		300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	10	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	650	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)**OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	600			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	3	4	5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 10A		0.25	0.29	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} , I _D = 10A		11		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		1500		pF
C _{oss}	Output Capacitance			350		pF
C _{rss}	Reverse Transfer Capacitance			35		pF
C _{oss eq.} (2)	Equivalent Output Capacitance	V _{GS} = 0V, V _{DS} = 0V to 400V		130		pF
R _g	Gate Input Resistance	f=1 MHz Gate DC Bias=0 Test Signal Level=20mV Open Drain		1.6		Ω

1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

2. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 200V, I_D = 10 A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		25		ns
t_r	Rise Time			20		ns
Q_g	Total Gate Charge	$V_{DD} = 400V, I_D = 20A,$ $V_{GS} = 10V$		39	54	nC
Q_{gs}	Gate-Source Charge			10		nC
Q_{gd}	Gate-Drain Charge			20		nC

SWITCHING OFF

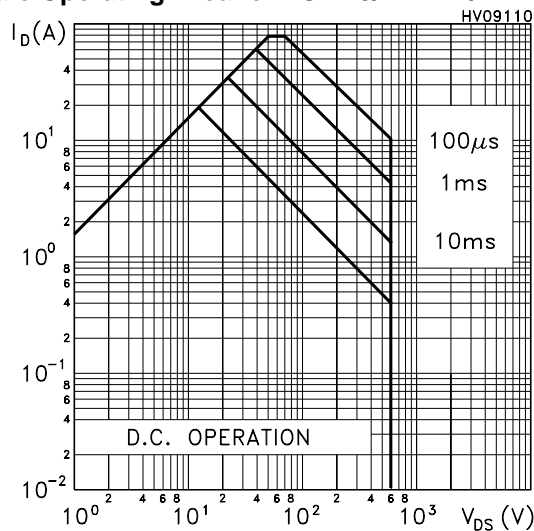
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_r(V_{off})$	Off-voltage Rise Time	$V_{DD} = 480V, I_D = 20 A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 5)		6		ns
t_f	Fall Time			11		ns
t_c	Cross-over Time			21		ns

SOURCE DRAIN DIODE

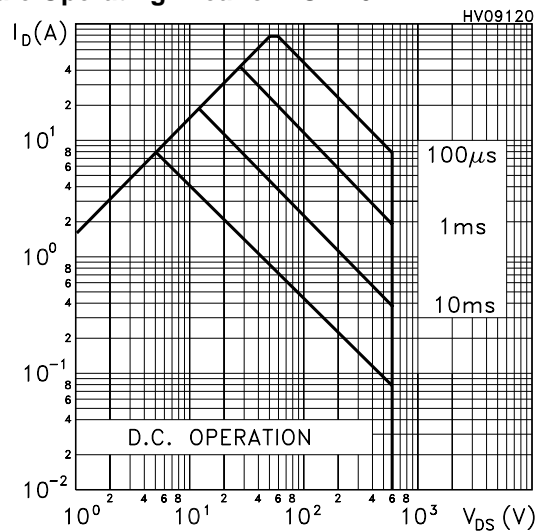
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				20	A
$I_{SDM} (2)$	Source-drain Current (pulsed)				80	A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 20 A, V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 20 A, di/dt = 100A/\mu s,$ $V_{DD} = 100 V, T_j = 25^\circ C$ (see test circuit, Figure 5)		390		ns
Q_{rr}	Reverse Recovery Charge			5		μC
I_{rrm}	Reverse Recovery Current			25		A
t_{rr}	Reverse Recovery Time	$I_{SD} = 20 A, di/dt = 100A/\mu s,$ $V_{DD} = 100 V, T_j = 150^\circ C$ (see test circuit, Figure 5)		510		ns
Q_{rr}	Reverse Recovery Charge			6.5		μC
I_{rrm}	Reverse Recovery Current			26		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

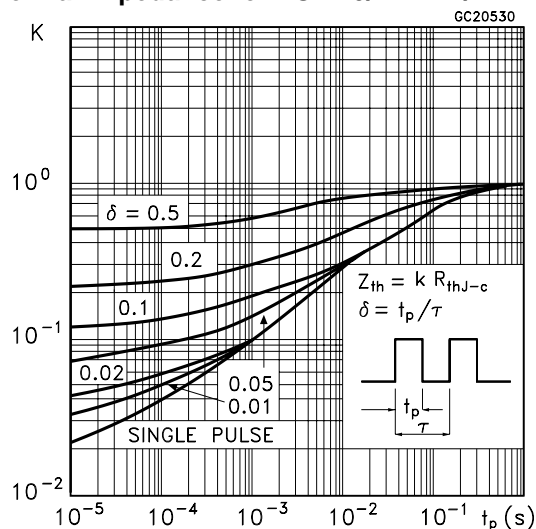
Safe Operating Area for TO-220/D2PAK/I2PAK



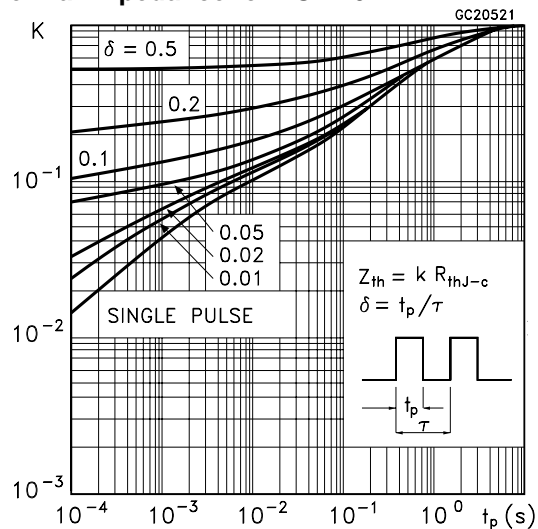
Safe Operating Area for TO-220FP



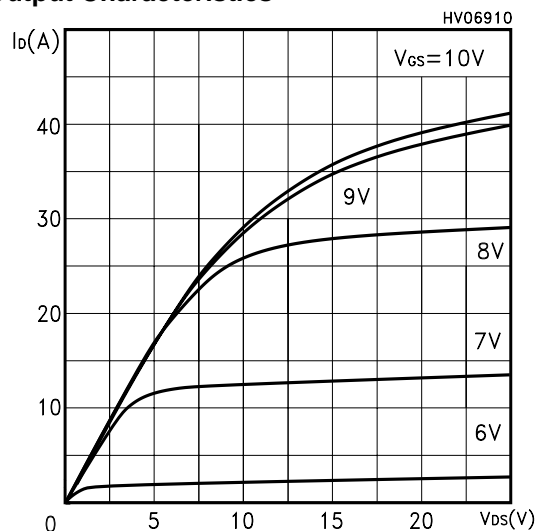
Thermal Impedance for TO-220/D2PAK/I2PAK



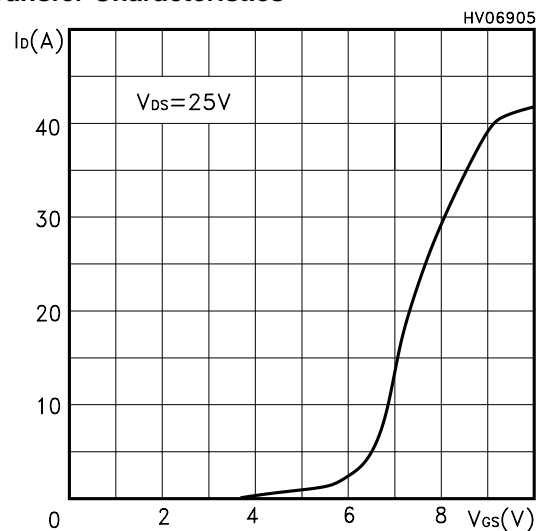
Thermal Impedance for TO-220FP



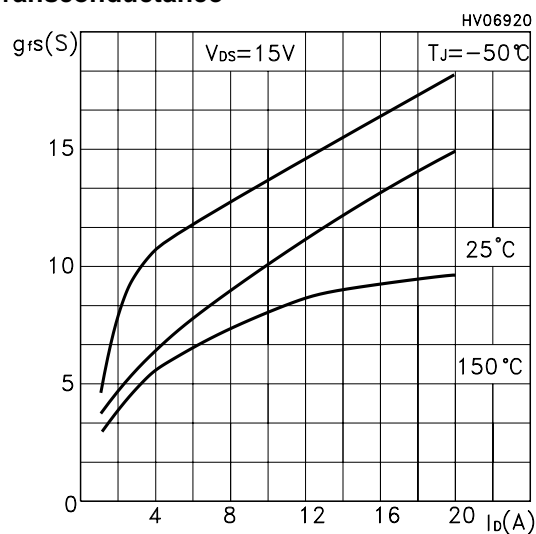
Output Characteristics



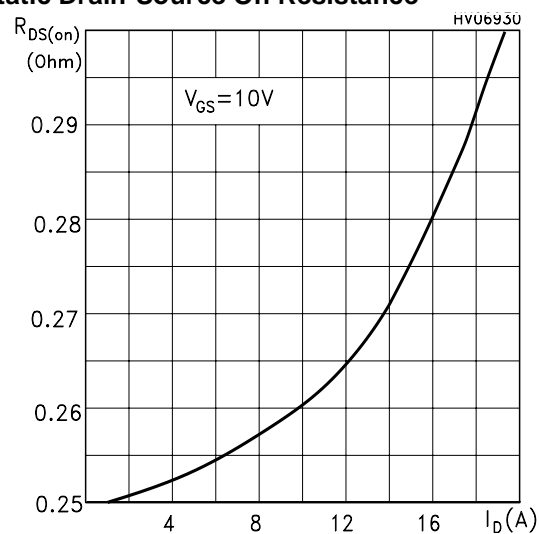
Transfer Characteristics



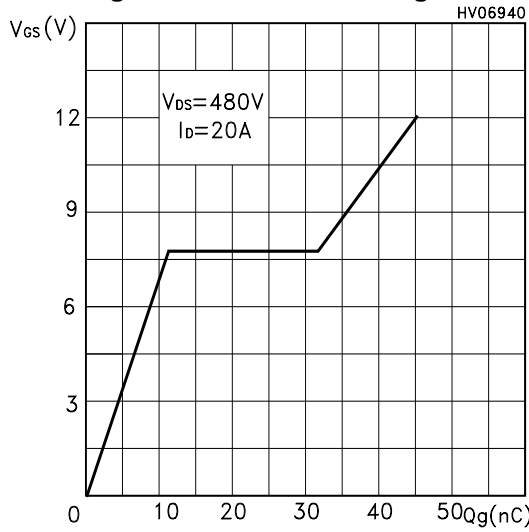
Transconductance



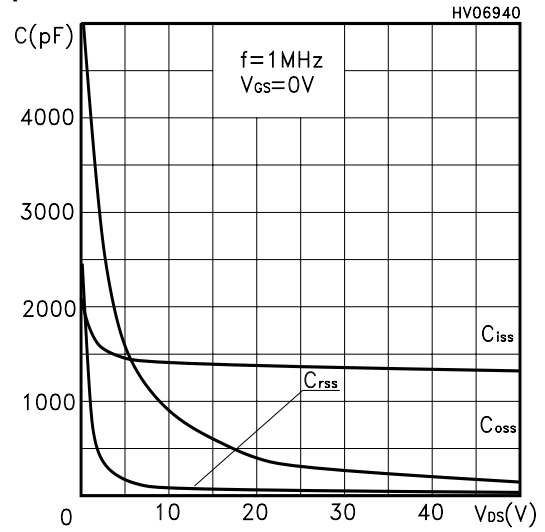
Static Drain-Source On Resistance



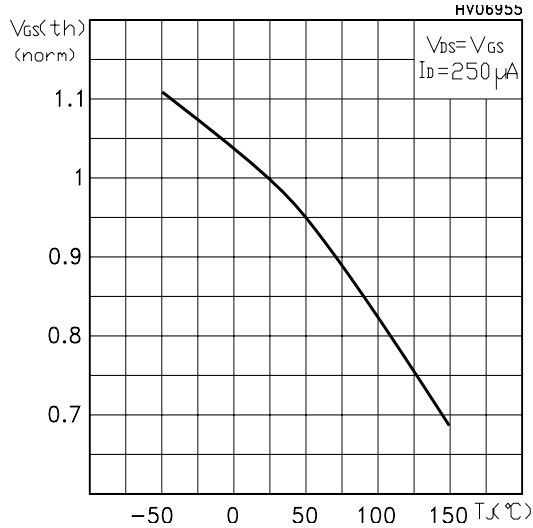
Gate Charge vs Gate-source Voltage



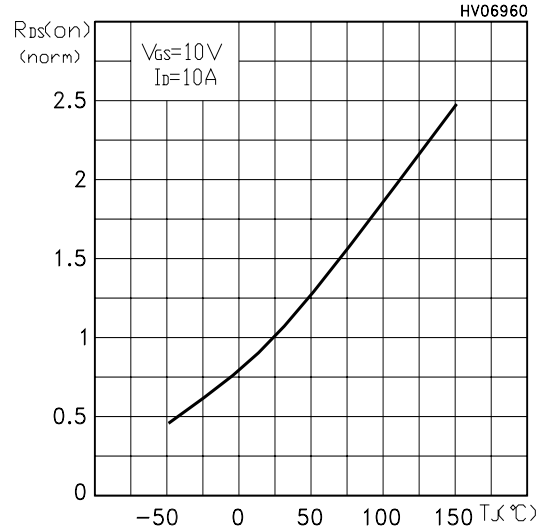
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

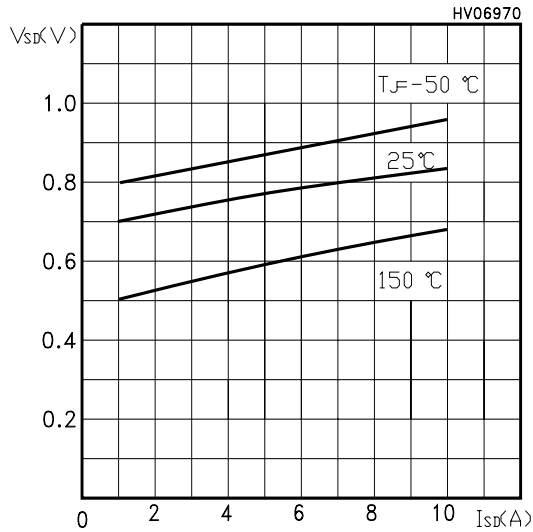


Fig. 1: Unclamped Inductive Load Test Circuit

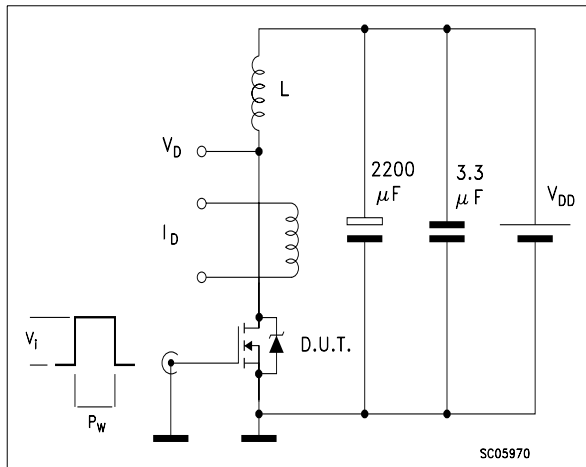


Fig. 2: Unclamped Inductive Waveform

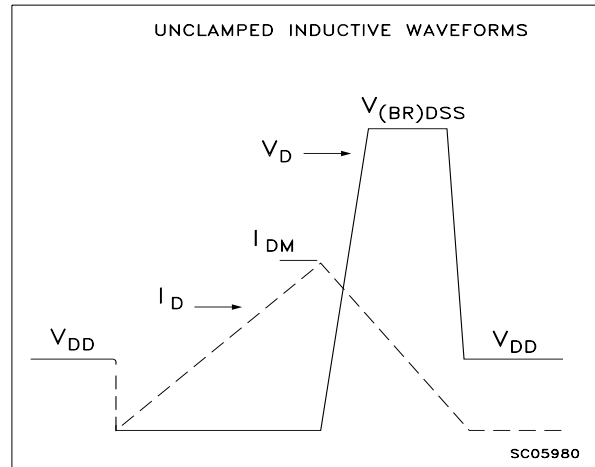


Fig. 3: Switching Times Test Circuit For Resistive Load

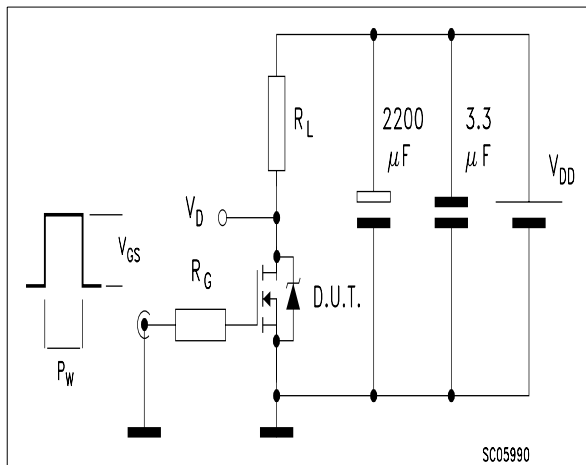


Fig. 4: Gate Charge test Circuit

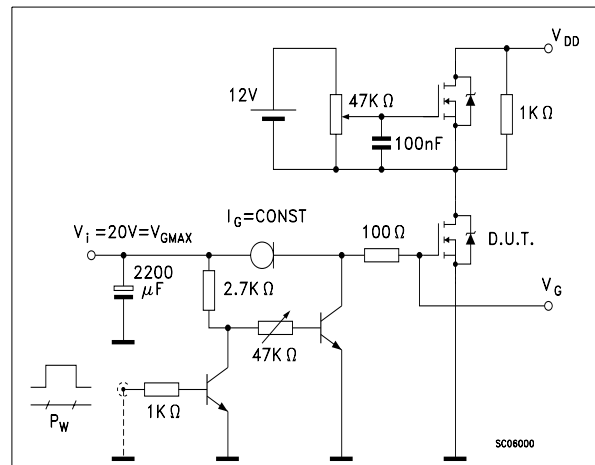
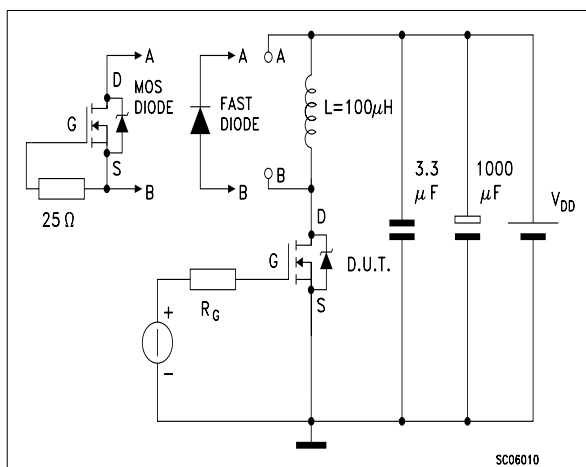
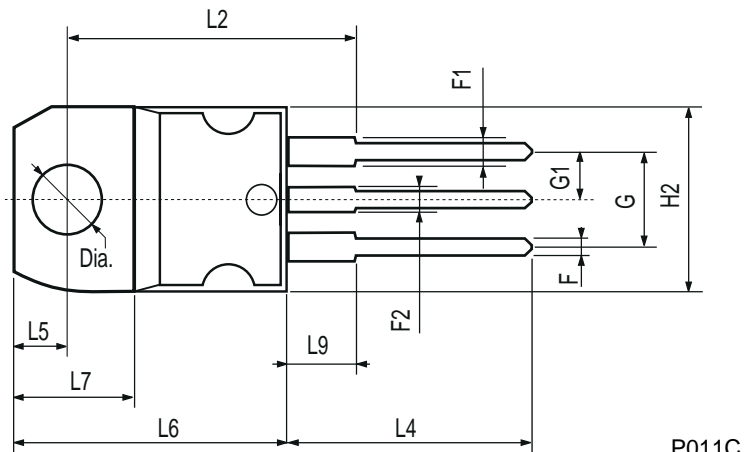
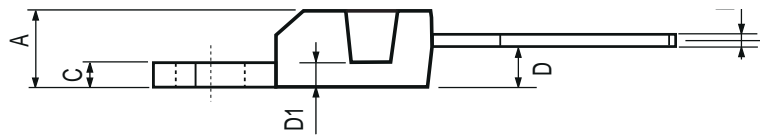


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-220 MECHANICAL DATA

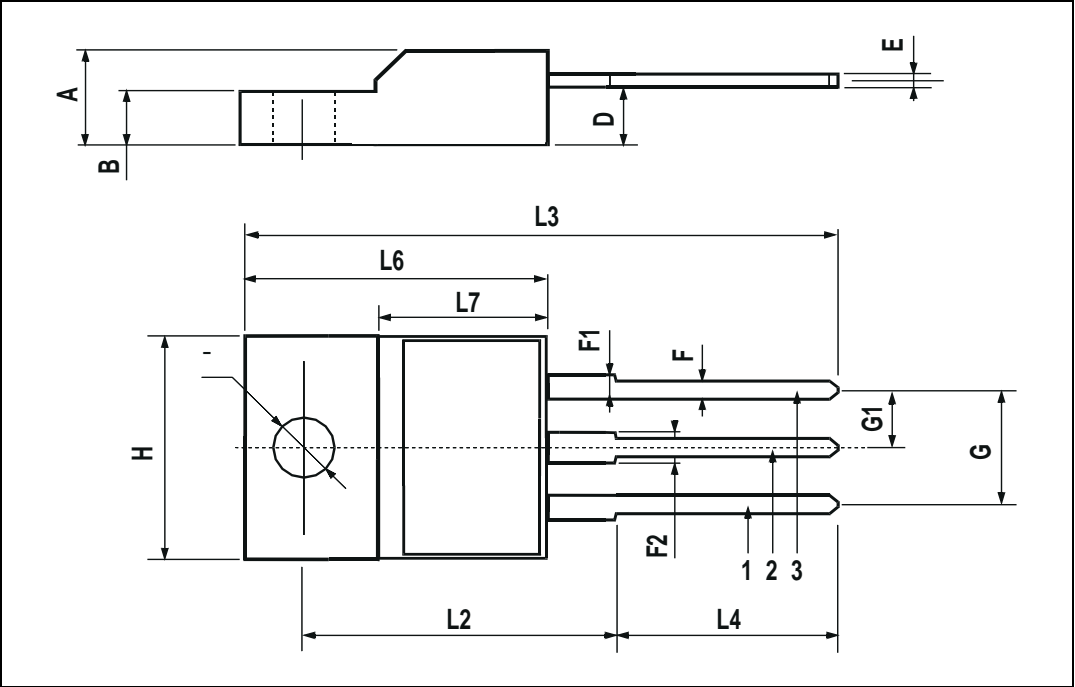
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



P011C

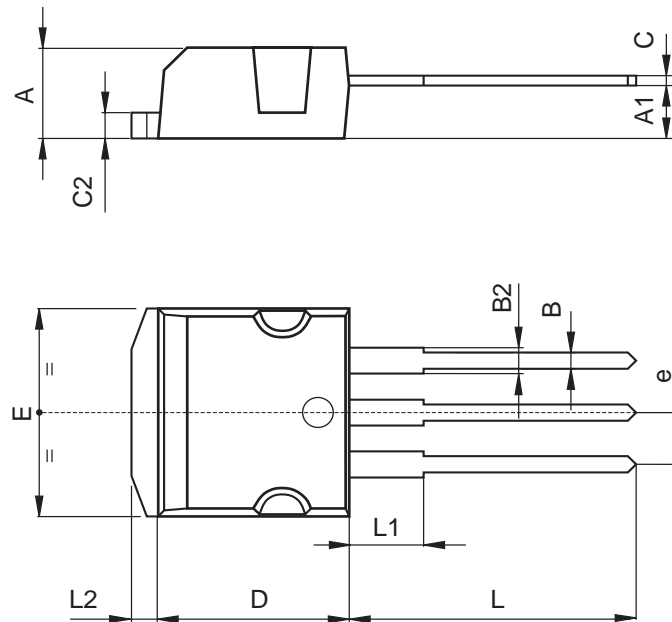
TO-220FP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-262 (I²PAK) MECHANICAL DATA

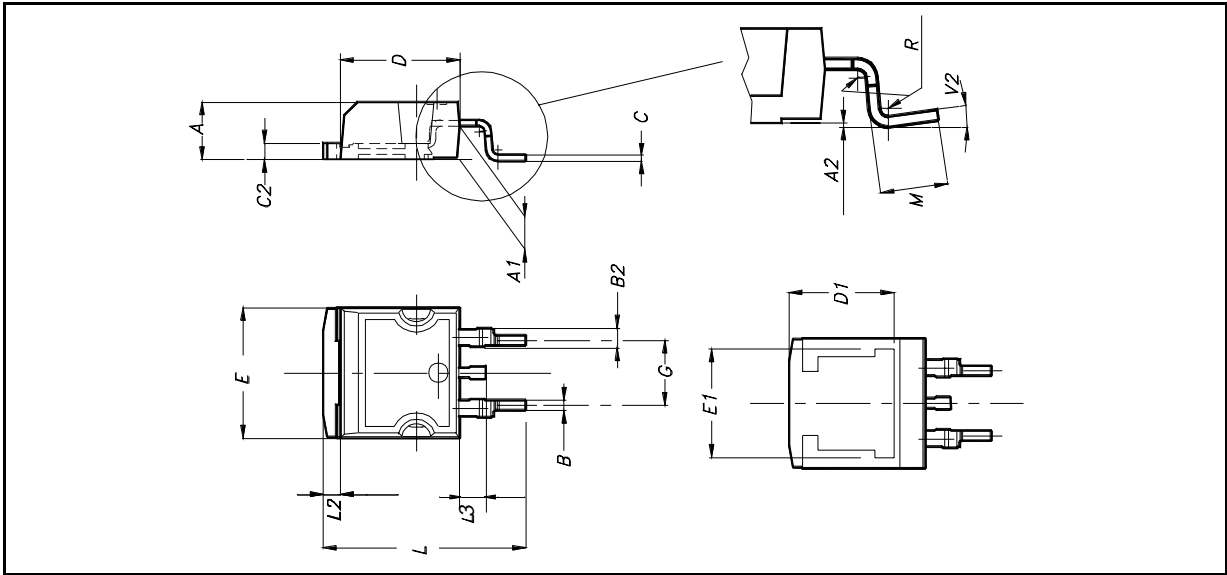
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
e	2.4		2.7	0.094		0.106
E	10		10.4	0.393		0.409
L	13.1		13.6	0.515		0.531
L1	3.48		3.78	0.137		0.149
L2	1.27		1.4	0.050		0.055



P011P5/E

D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°			



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